ABSTRACT OF THE DISCLOSURE

A frame transfer type solid-state imaging apparatus has a matrix of pixels which store information charges corresponding to a received image. The information charges are moved from the pixels to vertical transfer registers, and then to a horizontal transfer register, prior to being stored. A timing control circuit generates a vertical scan timing signal and a horizontal scan timing signal using a divided clock signal. A horizontal drive circuit generates a horizontal transfer clock using the divided clock signal and the horizontal scan timing signal. The horizontal transfer clock is used to move the information charges from the vertical transfer registers to the horizontal transfer register. A vertical drive circuit generates a vertical transfer clock using a reference clock signal and the vertical scan timing signal. The vertical transfer clock is used to move the information charges from the pixels to the vertical transfer registers. The divided clock signal is generated by dividing the reference clock signal by a predetermined ratio, such that the divided clock signal is longer than the reference clock signal. By generating the vertical transfer clock using the reference clock, and not the longer, divided clock, the resulting image does not have an increase in smear components.